THE CLAIMS

The following is a complete, clean listing of the claims with the status identifier in parentheses.

LISTING OF CLAIMS

1. (Previously Presented) A cache memory device for a digital signal processor (DSP), comprising:

a first cache memory for enabling a running flag signal in response to a given interrupt signal from a DSP core of the DSP to provide a given number of first instructions to the DSP core, and for disabling the running flag signal; and

a second cache memory for providing at least one second instruction to the DSP core when the running flag signal is disabled.

2. (Previously Presented) The cache memory device of claim 1, further comprising:

a first interface unit which interfaces the DSP core, first cache memory and second cache memory; and

a second interface unit which interfaces the first cache memory, second cache memory and a program memory that stores instructions for the DSP core.

3. (Previously Presented) The cache memory device of claim 1, wherein the given number of first instructions enable the DSP core to check a state of the interrupt request and to read relevant input variables.

4. (Previously Presented) The cache memory device of claim 2, wherein the first cache memory includes:

a cache memory block which stores a given one of the given number of first instructions received from the program memory in response to a corresponding write address and outputs each one of the given number of first instructions in response to a corresponding read address; and

a cache controller which generates the write address, read address, and a prefetch address using a program address received from the DSP core via the first interface unit, wherein the cache controller transmits the prefetch address to the program memory via the second interface unit in order to receive a given first instruction.

5. (Previously Presented) The cache memory device of claim 4, wherein the cache controller further includes:

a first register which receives the program address from the first interface unit and outputs the program address as a request address;

a second register which, in response to the interrupt signal sets a first received program address as a start address;

a third register which generates the prefetch address based on the start address;

a first subtraction unit which subtracts the start address from the request address to output the read address to the cache memory block;

a second subtraction unit which subtracts the start address from the prefetch address to output the write address to the cache memory block;

a hit/miss determination unit which outputs a hit signal if the read address is determined as valid, and which otherwise outputs a miss signal;

a counter which counts a number of times the hit signal is output, accumulates the count value and outputs the accumulated count value; and

a control signal generator which determines whether or not the number of times the hit signal is output reaches a threshold value based on the accumulated count value and enables the running flag signal when the number of times the hit signal is output reaches the threshold value.

6. (Previously Presented) The cache memory device of claim 5, wherein

the third register generates the prefetch address when the hit signal is output from the hit/miss determination unit, and

the prefetch address includes a plurality of addresses that continuously increase in value from the start address.

7. (Previously Presented) The cache memory device of claim 5, wherein the counter is reset when another interrupt signal is received.

8. (Previously Presented) The cache memory device of claim 5, wherein

the hit/miss determination unit outputs the miss signal if the read address output from the first subtraction unit is outside a given address range of the cache memory block or if the first instruction corresponding to the read address is invalid,

the control signal generator outputs a given control signal in response to the miss signal, and

the second register resets the start address in response to the control signal.

9. (Previously Presented) The cache memory device of claim 8, wherein

the second register stores the program address used to generate the read address that is outside the given address range and sets the stored program address as a new start address in response to the control signal, and

the third register transmits the new start address to the program memory in response to the control signal.

10. (Previously Presented) A method of controlling a cache memory device in a digital signal processor (DSP), comprising:

(a) first providing an instruction to a DSP core of the DSP from a cache memory, in response to a request from the DSP core;

(b) enabling a running flag signal in another cache memory in response to an interrupt signal received thereto from the DSP core;

(c) second providing, in response to a request from the DSP core, a given number of instructions from the another cache memory to the DSP core that are different from the first provided instruction; and

(d) disabling the running flag signal and ceasing said second providing step when the given number of instructions reaches a threshold value.

11. (Previously Presented) The method of claim 10, further comprising:

(e) repeating steps (a) through (d) iteratively until there are no further instruction requests from the DSP core.

12. (Previously Presented) The method of claim 10, wherein step (c) further includes:

(c1) generating a read address in response to a received program address;

(c2) outputting a miss signal and resetting a start address if the read address is not within a given address range, or if one of the given number of instructions corresponding to the read address is invalid;

(c3) transmitting the reset start address in order to receive a write instruction;

(c4) generating a write address based on the reset start address and storing the write instruction;

(c5) outputting a hit signal and the write instruction if the read address is within the given address range, or if the given instruction corresponding to the read address is valid;

(c6) counting a number of times the hit signal is output;

(c7) outputting an accumulated count value; and

(c8) iteratively repeating steps (c1) through (c6) to provide the given number of instructions, until a count value of the counting in step (c6) reaches a given value.

13. (Previously Presented) The method of claim 10, further comprising:

(f) determining whether or not the given number of instructions in step (c) reaches the given value based on the accumulated count value.

14. (Previously Presented) The method of claim 12, wherein step (c1) further includes:

(c11) setting a first received one of a plurality of received program addresses as a start address; and

(c12) generating the read address by subtracting the start address from a request address that represents a plurality of consecutively received program addresses.

15. (Previously Presented) The method of claim 12, wherein

the start address reset in step (c2) is the program address corresponding to the read address for which the miss signal is output, and

step (c4) further includes generating the write address by subtracting the reset start address from the received program address.

16. (Previously Presented) The method of claim 12, wherein step (c5) further includes:

(c51) generating a prefetch address using the start address;

(c52) generating a write address by subtracting the start address from the prefetch address; and

(c53) storing the write instruction corresponding to the prefetch address.

17. (Previously Presented) A cache memory device for a digital signal processor (DSP), comprising:

a first cache memory providing a first instruction in response to a program address received from a DSP core of the DSP, if there is no first instruction corresponding to the program address, and outputting a first miss signal;

a second cache memory providing at least one second instruction to the DSP core in response to a given interrupt signal and the first miss signal and, the second cache memory further disabling a running flag signal based after a given number of second instructions have been provided to the DSP core; and

a third cache memory which provides a third instruction to the DSP core in response to the first miss signal, when the running flag signal is disabled.

18. (Previously Presented) The cache memory device of claim 17, further comprising:

a first interface unit which interfaces the DSP core, first cache memory second cache memory and third cache memory; and

a second interface unit which interfaces the first cache memory, second cache memory, third cache memory and a program memory that stores instructions for the DSP core.

19. (Previously Presented) The cache memory device of claim 18, wherein the second cache memory includes:

a cache memory block which stores the second instructions, each second instruction received from the program memory in response to a corresponding write address, each second instruction output from the cache memory block in response to a corresponding read address; and

a cache controller which generates the write address, the read address, and a prefetch address using the program address received from the DSP core via the first

interface unit, the cache controller transmitting the prefetch address to the program memory via the second interface unit.

20. (Previously Presented) The cache memory device of claim 19, wherein the cache controller includes:

an input circuit which outputs the program address received in response to the first miss signal;

a first register which outputs the program address as a request address;

a second register which sets a first received program address as a start address in response to the interrupt signal;

a third register which generates the prefetch address using the start address;

a first subtraction unit which subtracts the start address from the request address to output the read address;

a second subtraction unit which subtracts the start address from the prefetch address to output the write address;

a hit/miss determination unit which outputs one of a hit signal and a second miss signal depending on a determination result;

a counter which counts the number of times the hit signal is output, accumulates the count value and outputs the accumulated count value; and

a control signal generator which enables the running flag signal in response to the interrupt signal and disables the running flag signal, if the accumulated count value reaches the threshold value.

21. (Previously Presented) The cache memory device of claim 20, wherein

the determination result outputs the second miss signal when the read address is not within a given address range of the cache memory block or the second instruction corresponding to the read address is invalid,

the control signal generator outputs a given control signal in response to the second miss signal,

the second register resets the start address in response to the control signal, and

the third register generates the prefetch address using the start address, which has been reset in response to the control signal.

22. (Previously Presented) A method of controlling a cache memory device in a digital signal processor (DSP), comprising:

(a) first providing a first instruction from a first cache memory to a DSP core in response to a program address received from the DSP core;

(b) second providing at least one second instruction from a second cache memory to the DSP core in response to the program address based on at least one of an output of a first miss signal from the first cache memory and an enabling of a running flag signal by the second cache memory;

(c) disabling the running flag signal and ceasing step (b) when a number of second instructions provided to the DSP core reaches a given value;

(d) third providing a third instruction from a third cache memory to the DSP core in response to the program address based on at least one the first miss signal output from the first cache memory and a disabling of the running flag signal by the second cache memory;

(e) enabling the running flag signal at the second cache memory when an interrupt signal is received thereto from the DSP core.

23. (Previously Presented) The method of claim 22, further comprising:

(f) iteratively repeating steps (a) through (e) until there are no further instruction requests received from the DSP core.

24. (Previously Presented) The method of claim 22, wherein step (b) includes:

(b1) generating a read address from a program address;

(b2) outputting a second miss signal and resetting a start address if the read address is not within a given address range or if the second instruction corresponding to the read address is invalid;

(b3) transmitting the reset start address to receive a second write instruction to be stored;

(b4) generating a write address based on the reset start address and storing a second write instruction;

(b5) outputting a hit signal and the second instruction if the read address is within a given address range or if the second instruction corresponding to the read address is valid;

(b6) counting the number of times the hit signal is output; and

(b7) iteratively repeating steps (b1) through (b6) until a count value of the counting in step (b6) reaches a given value.

25. (Previously Presented) A cache memory device for a digital signal processor (DSP) that is controlled in accordance with the method of claim 10.

26. (Previously Presented) A cache memory device for a digital signal processor (DSP) that is controlled in accordance with the method of claim 22.